Decoupling Capacitor Induced Bandwidth and Delay expressions for On-Chip RLC global interconnects

Santosh Ku Chhotray, Sandeep Ku Dash, Subhakanta Swain, Mrigendra Kumar, Nivedita Rout

Abstract—Continuously scaling down devices is the main goal in deep sub-micron (DSM) technology. Though using DSM technology we are achieving many advantages. But circuit performances are badly affected because of secondary effects like crosstalk noise. According to International Technical Roadmap for Semiconductors (ITRS) 2011 report today’s DSM technology outsmarted Moore’s law to work in a new industrial trend called “More than Moore” (MtM). To accomplish this, it is necessary to analyze the timing behavior of the interconnect. Decoupling capacitor can have significant effect on principal characteristics of an integrated circuit (IC) i.e. speed, cost and power. So by including a decoupling capacitor intentionally can control secondary effects in very deep sub-micron (VDSM) technology. But inserting a decoupling capacitor affects delay and bandwidth of the interconnect. So while inserting decoupling capacitor we have to check for the disturbances in delay and bandwidth. Here in this paper two expressions for calculating delay and bandwidth have derived.

Keywords—Decoupling capacitor, interconnects, Bandwidth, Delay

I. Introduction

An electronic system consists of 2 parts: the basic components (transistor, diode, passive circuit elements, MEMS etc.) and the highly complex interconnect fabric linking them (from local to global in a hierarchical manner). As global interconnects are responsible for power supply, so any disturbance in global interconnect can affect a lot to signal propagation along it and the victim (idle) interconnect. Circuit integration densities rise with each very deep sub-micron (VDSM) due to smaller devices and larger dies. By using VDSM technology we are achieving many advantages. Again to handle high speed and low power in VDSM technology we intentionally add decoupling capacitors to interconnect line. But these decoupling capacitors show some unexpected results because of secondary effects like crosstalk noise. Because of crosstalk functional and timing problems arises like delay, bandwidth etc. Several factors bound to VDSM technology like density of integration, no. of metal layers etc are reason behind these unexpected outcomes. RC modelling is not enough for global interconnection at high frequencies. Working in VDSM technology we cannot ignore wire resistances, capacitances and inductances. So to handle this two-fold nature of VDSM technology here in our proposed model we focus on global interconnects where we consider wire resistances, inductances and practical decoupling capacitances. The timing parameters like propagation delay and bandwidth depends on power supply level during the signal transition. Various techniques have been proposed for the delay analysis of global interconnects. Here in this paper the crosstalk effects because of capacitive coupling and inductive coupling are considered on different nodes of global interconnects. Then using derived expression delay and bandwidths are calculated and compared with 180nm HSpice technology.

II. Decoupling capacitor effects

Decoupling capacitors are often utilized to manage the power supply noise. Due to importance of decoupling capacitors in current and future ICs, significant research has been developed over past several decades. To be effective, the decoupling capacitor should satisfy two requirements. First, the capacitor should have sufficient capacitance to store a significant amount of energy. Second, to supply sufficient power at high frequency, the capacitor should be able to release and accumulate energy at high rate.

III. Proposed Model

![Proposed model with decoupling capacitor](image)

Figure 1 Proposed model with decoupling capacitor

Above figure shows two interconnect lines connected by a decoupling capacitor. At high frequency as the frequency increases, the impedance of the decoupling capacitor increases linearly with frequency as shown in fig. 2. This increase in the impedance of a practical decoupling capacitance is due to the...
parasitic inductance of the decoupling capacitor. The parasitic inductance is referred to as the Effective Series Inductance (ESL). The impedance of a decoupling capacitor reaches minimum impedance at frequency \( \omega = \frac{1}{\sqrt{LC}} \) to get negligible disturbance in delay and bandwidth. Effective Series Resistance (ESR) of a decoupling capacitor is the minimum impedance of the decoupling capacitor.

Figure 2 Frequency Vs Impedance plot for high frequency interconnect

Proposed estimation method separates the victim (idle) net and the aggressor net into two equivalent circuits. The aggressor is modeled as shown in Fig. 3 and victim line is modeled as shown in Fig. 4.

\begin{align*}
V_{agg}(t) &= \begin{cases} 
\frac{t}{\tau_a}V_{dd} & 0 < t < \tau_a \\
V_{dd} & t > \tau_a 
\end{cases} \\
V_{agg}(s) &= \frac{1}{s^2\tau_a}V_{dd}
\end{align*}

It can be represented in S-domain as

Here for simplicity we have taken \( V_{dd}=1 \).

Proposed model is based on the above circuit shown in Fig. 5. Figure represents victim line parameters and \( V_{out}(S) \) is the coupled voltage of decoupling capacitor.
Now applying KVL to loop L1
\[-\frac{I}{C_v S} + L_v S(I - I_1) + R_v (I - I_1) = 0\]
\[
(\frac{1}{C_v S} + L_v S + R_v) I_1 = I(L_v S + R_v)
\]
\[
I = \frac{(\frac{1}{C_v S} + L_v S + R_v) I_1}{(L_v S + R_v)}
\]
(3)

Now applying KVL to loop L2
\[V_{agg}(S) - RI - LSI - \frac{I}{C_v S} - R_v (I - I_1) - L_v S(I - I_1) = 0\]
\[V_{agg}(S) - I(R + LS + \frac{1}{C_v S} + R_v + L_v S) + (L_v S + R_v) I_1 = 0\]

Now using (3)
\[V_{agg}(S) = \frac{(\frac{1}{C_v S} + L_v S + R_v) I_1}{(L_v S + R_v)} (R + LS + \frac{1}{C_v S} + R_v + L_v S) + (L_v S + R_v) I_1\]
Now simplifying above equation
\[I_1(S) = \frac{V_{agg}(S)(L_v C_v S^2 + R_v C_v S)}{C_v S(L_v C_v S^2 + R_v C_v S + 1)(R C_v S + R_v C_v S + L C_v S^2 + L_v C_v S^2) - (R_v + C_v S)(L_v C_v S^2 + R_v C_v S)C_v S}
\]
\[V_{out}(S) = \frac{I_1}{C_v S}
\]
(5)

Now using (4) in (5) and rearranging
\[V_{out}(S) = \frac{C_v S(L_v C_v S^2 + R_v C_v S)}{C_v S(L_v C_v S^2 + R_v C_v S + 1)(R C_v S + R_v C_v S + L C_v S^2 + L_v C_v S^2) - (R_v + C_v S)(L_v C_v S^2 + R_v C_v S)C_v S}
\]

Considering dominating pole and ignoring higher order terms
\[V_{out}(S) = \frac{j C_v L_v C_v \omega + R_v C_v C_v}{R C_v C_v + R_v C_v C_v}
\]

Applying modulus on both sides and equating to \(\frac{1}{\sqrt{2}}\)
\[\frac{1}{\sqrt{2}} = \sqrt{(C_v L_v C_v \omega)^2 + (R_v C_v C_v)^2}
\]
\[
\frac{1}{\sqrt{2}} = \frac{1}{\sqrt{2}} \frac{(R C_v C_v + R_v C_v C_v)^2}{R C_v C_v + R_v C_v C_v}
\]
\[
\omega^2 = \frac{1}{(RC_v C_v + R_v C_v C_v)^2 - (R_v C_v C_v)^2}
\]
\[
\omega = \frac{1}{2 \pi} \sqrt{\frac{RC_v + R_v C_v}{\sqrt{2} L_v C_v}} = \frac{R_v}{L_v}
\]
(6)

8. Delay Calculation

For calculation of delay we consider 50% rise time when \(V_{out}(t) = 0.5V_{dd}\)

From (5) we can get delay expression as
\[V_{out}(S) = \frac{0.5V_{dd}}{S}
\]

Using above value in (7)
\[0.5V_{dd} = \frac{V_{dd}}{S \tau_d} C_v S(L_v C_v S^2 + R_v C_v S)
\]
\[S \tau_d = \frac{C_v S(L_v C_v S^2 + R_v C_v S + 1)(R C_v S + R_v C_v S + L C_v S^2 + L_v C_v S^2) - (R_v + C_v S)(L_v C_v S^2 + R_v C_v S)C_v S}{C_v S(L_v C_v S^2 + R_v C_v S + 1)(R C_v S + R_v C_v S + L C_v S^2 + L_v C_v S^2) - (R_v + C_v S)(L_v C_v S^2 + R_v C_v S)C_v S}
\]

Now for delay calculation equating \(V_{out}(t) = 0.5V_{dd}\)
\[V_{out}(S) = \frac{0.5V_{dd}}{S}
\]

Now taking inverse Laplace transform and solving
\[t_{50\%} = 1.18 \sqrt{3X^2 - 2Y}
\]

Where
\[X = R(C_v + C_v) + R_v C_v - \frac{R_v}{L_v}
\]

And
\[Y = R R_v C_v C_v + \frac{R_v^2 C_v}{L_v} - R_v C_v
\]
iv. Simulation Result and Discussion

Our experimentd high-speed interconnect system consist of two coupled interconnect lines of length \( d=100 \) um. The extracted values for the parameters \( R \), \( L \), and \( C \) are given in Table 1.

<table>
<thead>
<tr>
<th>Parameter(s)</th>
<th>Value/m</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resistance(( R ))</td>
<td>120 k( \Omega )/m</td>
</tr>
<tr>
<td>Inductance(( L ))</td>
<td>270 nH/m</td>
</tr>
<tr>
<td>Coupling Capacitance(( C_c ))</td>
<td>681.23 pF/m</td>
</tr>
<tr>
<td>Capacitance(( C ))</td>
<td>240 pF/m</td>
</tr>
</tbody>
</table>

Table II compares the bandwidth we got by proposed model with the values from SPICE simulator for different source resistances. With the varying source resistance we got different values of bandwidth with approximately 3.881\% of error.

<table>
<thead>
<tr>
<th>( R_s (\Omega) )</th>
<th>( L_s (pH) )</th>
<th>( C_c (pF) )</th>
<th>SPICE Bandwidth (MHz)</th>
<th>Proposed Model (MHz)</th>
<th>% Error</th>
</tr>
</thead>
<tbody>
<tr>
<td>45</td>
<td>2.5</td>
<td>0.175</td>
<td>20.14</td>
<td>20.05</td>
<td>0.4468</td>
</tr>
<tr>
<td>95</td>
<td>2.5</td>
<td>0.175</td>
<td>41.55</td>
<td>41.35</td>
<td>0.4813</td>
</tr>
<tr>
<td>445</td>
<td>2.5</td>
<td>0.175</td>
<td>221.36</td>
<td>220.03</td>
<td>0.6008</td>
</tr>
<tr>
<td>995</td>
<td>2.5</td>
<td>0.175</td>
<td>465.13</td>
<td>462.01</td>
<td>0.6707</td>
</tr>
</tbody>
</table>

Table III compares the delay we got using derived expression with SPICE simulator values and the average percentage of error is about 0.5499\%.

<table>
<thead>
<tr>
<th>( R_s (\Omega) )</th>
<th>( L_s (pH) )</th>
<th>( C_c (pF) )</th>
<th>SPICE Delay(ps)</th>
<th>Proposed Model(ps)</th>
<th>% Error</th>
</tr>
</thead>
<tbody>
<tr>
<td>45</td>
<td>2.5</td>
<td>0.175</td>
<td>20.1</td>
<td>20.0</td>
<td>0.4468</td>
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<td>95</td>
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<tr>
<td>445</td>
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<td>465.2</td>
<td>462.0</td>
<td>0.6707</td>
</tr>
</tbody>
</table>

v. Conclusion

In this study simple and explicit analytical expressions have been proposed for calculating delay and bandwidth for global interconnects in very deep sub-micron (VDSM) technology where we consider decoupling capacitors for controlling signal timing behavior. It is expected that these expressions will also applicable to 90nm and 45nm technology and to be used efficiently in high speed and large scale circuits. Hence these closed form expressions can be implemented in VLSI design tool for efficient modeling of interconnection in high speed VLSI chips. These analytical delay formulas are much faster than simulating using SPICE. So can save time and of course the cost of using expensive tools like SPICE. In future we will try to simplify these equations to simpler form as possible.
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References


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